IN THE CLAIMS

Please cancel claims 12 and 24 without prejudice and amend the remaining claims as follows:

1. (Currently Amended) In a data processing system having a first processor with a first software architecture, the improvement comprising:

a. a plurality of emulation objects each executable by said first processor wherein each of said emulation objects emulates operation of a different one of a plurality of target processors each of said plurality of target processors having a plurality of specialized communication instructions wherein each of said plurality of target processors has a software architecture different from said first software architecture.

2. (Original) An improvement according to claim 1 wherein each of said emulation object is compatible with said first software architecture.

3. (Original) An improvement according to claim 2 wherein at least one of said plurality of emulation objects further comprises an array of procedures compatible with said first software architecture and a list of instructions compatible with a second software architecture.

4. (Currently Amended) In a data processing system having a first processor with a first software architecture, the [[an]] improvement ~~according to claims 3~~ comprising:

a. a plurality of emulation objects each executable by said first processor wherein each of said emulation objects emulates operation of a different one of a plurality of target processors wherein each of said plurality of target processors has a software architecture different from said first software architecture;

b. wherein each of said emulation object is compatible with said first software architecture;

c. wherein at least one of said plurality of emulation objects further comprises an array of procedures compatible with said first software architecture and a list of instructions compatible with a second software architecture; and

d. wherein said list of instructions includes specialized instructions for communications processing.

5. (Original) An improvement according to claim 4 wherein each of said array of procedures corresponds to a one of said list of instructions through the use of an operation code and corresponding four bit field.

6. (Currently Amended) An apparatus comprising:

a. a first instruction processor having a first software architecture; and

b. a plurality of emulation objects responsively coupled to said first instruction processor wherein each of said plurality of emulation objects permits said first instruction processor to emulate a different one of a plurality of target processors and wherein each of said plurality of target processors has a software architecture different from said first software architecture and wherein said different software architecture includes at least one specialized communication instruction.

7. (Original) An apparatus according to claim 6 further comprising a first computer program having a first plurality of instructions which are compatible with said first software architecture.

8. (Currently Amended) An apparatus ~~according to claim 7~~ comprising:

a. a first instruction processor having a first software architecture;

b. a plurality of emulation objects responsively coupled to said first instruction processor wherein each of said plurality of emulation objects permits said first instruction processor to

emulate a different one of a plurality of target processors and wherein each of said plurality of target processors has a software architecture different from said first software architecture;

c. a first computer program having a first plurality of instructions which are compatible with said first software architecture; and

d. wherein said first plurality of instructions further comprises a specialized communication instruction.

9. (Original) An apparatus according to claim 8 wherein a first one of said emulation objects further comprises an array of procedures and a list of instructions.

10. (Original) An apparatus according to claim 9 wherein each of said procedures of said array of procedures is directly linked to a different one of said list of instructions.

11. (Currently Amended) A method of emulating a plurality of target processors by a first processor having a first software architecture incompatible with the software architectures of said plurality of target processors, the method comprising:

a. executing a first emulation object corresponding to a first of said plurality of target processors; ~~and~~

b. executing another emulation object corresponding to another of said plurality of target processors; and

c. wherein said first emulation object further comprises a specialized instruction.

12. (Canceled)

13. (Currently Amended) A method ~~according to claim 12~~ of emulating a plurality of target processors by a first processor having a first software architecture incompatible with the software architectures of said plurality of target processors, the method comprising:

a. executing a first emulation object corresponding to a first of said plurality of target processors;

b. executing another emulation object corresponding to another of said plurality of target processors;

c. repeating step b for each of said plurality of target processors; and

d. wherein said first emulation object further comprises a specialized instruction.

14. (Original) A method according to claim 13 wherein said specialized instruction further comprises an instruction for communication processing.

15. (Original) A method according to claim 14 wherein said first emulation object further comprises an array of procedures.

16. (Currently Amended) An apparatus comprising:

a. executing means having a first software architecture for executing computer instructions compatible with said first software architecture; and

b. containing means responsively coupled to said executing means for containing a plurality of emulation objects wherein each of said plurality of emulation objects corresponds to a different one of a plurality of target processors and each of said plurality of target processors has a software architecture which is incompatible with said first software architecture.

17. (Original) An apparatus according to claim 16 wherein a first of said emulation objects further comprises an array of procedures.

18. (Original) An apparatus according to claim 17 wherein said first of said emulation objects further comprises a list of instructions wherein each of said array of procedures corresponds to a different one of said list of instructions.

19. (Original) An apparatus according to claim 18 wherein at least one of said list of instructions further comprises a communication processing instruction.

20. (Original) An apparatus according to claim 19 wherein said list of instructions further comprises a plurality of communication processing instructions.

21. (Currently Amended) An apparatus comprising:

a. a first instruction processor which executes a first sequence of instructions in accordance with a first software architecture;

b. a second sequence of instructions in accordance with a second software architecture which is incompatible with said first software architecture and wherein one of said second sequence of instructions further comprises an instruction for communications processing;

c. a plurality of emulation objects wherein a first of said plurality of emulation objects corresponds to said second software architecture;

d. a plurality of ~~short~~ sequences of target instructions in accordance with said first software architecture located within said first of said plurality of emulation objects wherein said

one of said second sequence of instructions corresponds to one of said plurality of ~~short~~ sequences of target instructions; and

c. a selection facility which selects said one of said plurality of ~~short~~ sequences of target instructions for presentation to said first instruction processor for execution.

22. (Currently Amended) An apparatus according to claim 21 wherein said selection facility utilizes a portion of said one of said second sequence of instructions to select said one of said plurality of ~~short~~ sequences of target instructions.

23. (Original) An apparatus according to claim 22 wherein said portion further comprises an op code.

24. (Canceled)

25. (Currently Amended) An apparatus ~~according to claim 24~~ comprising:

a. a first instruction processor which executes a first sequence of instructions in accordance with a first software architecture;

b. a second sequence of instructions in accordance with a second software architecture which is incompatible with said first software architecture;

c. a plurality of emulation objects wherein a first of said plurality of emulation objects corresponds to said second software architecture;

d. a plurality of sequences of target instructions in accordance with said first software architecture located within said first of said plurality of emulation objects wherein one of said second sequence of instructions corresponds to one of said plurality of sequences of target instructions;

c. a selection facility which selects said one of said plurality of sequences of target instructions for presentation to said first instruction processor for execution;

d. wherein said selection facility utilizes a portion of said one of said second sequence of instructions to select said one of said plurality of sequences of target instructions;

c. wherein said portion further comprises an op code;

e. wherein said op code points to said one of said plurality of sequences of target instructions; and

f. wherein said one of said second sequence of instructions further comprises an instruction for communications processing.